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10/807,327	03/24/2004	Takashi Ando	042271	4003

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,327	ANDO, TAKASHI	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *13-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the election filed September 26, 2005.

Election/Restrictions

2. Applicant's election without traverse of Embodiment I in the reply filed on 9/26/05 is acknowledged.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The specification is objected to as failing to provide proper antecedent basis for the following claimed subject matter: a) the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor (See Claims 5 and 6); and b) the line connecting the source and the drain of one of said two transistors is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor (See Claims 7 and 8). See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction is required.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: a) 33 (Figure 3); b) 10 (Figure 5); c) 71 (See Figure 10); d) 51, 53-56, 58-68 (Figure 11); and e) 52 (Figure 12). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s): a) the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor (See Claims 5 and 6); b) the line connecting the source and the drain of one of said two transistors is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor (See Claims 7 and 8); and c) extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claims 5 and 6 are objected to because of the following informalities: a) it appears that "is substantially" should read "substantially" (See Claims 5 and 6). Appropriate correction is required.

Information Disclosure Statement

8. The information disclosure statement filed 3/24/04 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 2-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "located at substantial central point of a minimal rectangular shape made by four ferroelectric capacitors out of said plurality of ferroelectric capacitors" (See Claim 2); and b) "extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors" (See Claims 3 and 4). Claims 5-12 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Summerfelt et al. (U.S. Publication No. 2005/0012125).

In regards to claim 1, Summerfelt et al. ("Summerfelt") discloses the following:

a) a semiconductor substrate (4) (For Example: See Figure 1A);

b) a plurality of transistors formed on a surface of said semiconductor substrate (For Example: See Figure 1A);

c) an interlayer insulating film (14) for covering said transistors (For Example: See Figure 1A);

d) a plurality of ferroelectric capacitors (C) formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain (6) of said transistor via a first contact plug (16),wherein said plurality of ferroelectric capacitors are arranged in an array, wherein each of said plurality of ferroelectric capacitor has substantially a rectangular planar shape (See Figure 1A and 1C) (Note: Merriam-Webster defines substantial as being "largely but not wholly that which is specified."); and

e) the ratio between the length of a long side of the rectangular shape and the distance between the long sides of two ferroelectric capacitors adjacent to each other substantially coincides with the ratio between the length of a short side of the rectangular shape and the distance between the short sides of two ferroelectric capacitors adjacent to each other (For Example: See Figure 1C) (Note: Merriam-Webster defines substantial as being "largely but not wholly that which is specified.").

13. Claim 2, as far as understood, is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Prior Art.

In regards to claim 2, Applicant's Prior Art discloses the following:

a) a semiconductor substrate (51) (For Example: See Figure 11);

b) a plurality of transistors formed on a surface of said semiconductor substrate (For Example: See Figure 11);

c) an interlayer insulating film (58) for covering said transistors (For Example: See Figure 11);

d) a plurality of ferroelectric capacitors (65) formed over said interlayer insulating film, an electrode of each of said plurality of ferroelectric capacitors being connected to one of a source or a drain (56) of said transistor via a first contact plug (59),wherein said plurality of ferroelectric capacitors are arranged in an array, (For Example: See Figure 11);

e) a plurality of bit lines (61) formed over said interlayer insulating film, each of said plurality of bit lines being connected to the other one of the source or the drain of said transistor via a second contact plug (60) (For Example: See Figure 11); and

f) the first contact plug is located at substantial central point of a minimal rectangular shape made by four ferroelectric capacitors out of said plurality of ferroelectric capacitors (For Example: See Figure 10).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 3, 5 and 9, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Summerfelt et al. (U.S. Publication No. 2005/0012125).

In regards to claim 3, Summerfelt fails to disclose the following:

a) a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors.

However, the applicant has not established the critical nature of "a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

In regards to claim 5, Summerfelt discloses the following:

a) an element isolation insulating film (8) formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor (For Example: See Figure 1A).

In regards to claim 9, Summerfelt discloses the following:

a) the other one of the source or the drain of said transistor is shared by said two transistors in each element region (For Example: See Figure 1A).

16. Claim 4, as far as understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art.

In regards to claim 4, Summerfelt fails to disclose the following:

a) a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors.

However, the applicant has not established the critical nature of "a straight line connecting the source and the drain of said transistor extends in a direction substantially inclined at an angle of 45 degrees to longitudinal and lateral directions of the arrays constituted by the plurality of ferroelectric capacitors." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges.

17. Claims 6 and 10, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Summerfelt et al. (U.S. Publication No. 2005/0012125).

In regards to claim 6, Applicant's Prior Art fails to disclose the following:

a) an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor.

However, Summerfelt discloses a semiconductor device that has an element isolation insulating film (8) formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors, and wherein the line connecting the source and the drain of one of said two transistors is substantially coincides with the line connecting the source and the drain of the other one of said two transistor as disclosed in Summerfelt because it aids in separating the transistors source/drains (For Example: See Paragraph 29).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 10, Applicant's Prior Art fails to disclose the following:

a) the other one of the source or the drain of said transistor is shared by said two transistors in each element region.

However, Summerfelt discloses a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region as disclosed in Summerfelt because it aids in reducing the capacitance (For Example: See Paragraphs 7 and 8).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

18. Claims 7 and 11, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Summerfelt et al. (U.S. Publication No. 2005/0012125) in view of Corvasce et al. (U.S. Patent No. 6,656,801).

In regards to claim 7, Summerfelt discloses the following:

a) an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors (For Example: See Figure 1A).

In regards to claim 7, Summerfelt fails to disclose the following:

a) the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor.

However, Corvasce et al. ("Corvasce") discloses a semiconductor device that has the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Summerfelt to include a semiconductor device that has the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor as disclosed in Corvasce because it aids in providing minimal cell size (For Example: See Abstract).

Additionally, since Summerfelt and Corvasce are both from the same field of endeavor, the purpose disclosed by Corvasce would have been recognized in the pertinent art of Summerfelt.

In regards to claim 11, Summerfelt discloses the following:

a) the other one of the source or the drain of said transistor is shared by said two transistors in each element region (For Example: See Figure 1A).

19. Claims 8 and 12, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art in view of Summerfelt et al. (U.S. Publication No. 2005/0012125) and Corvasce et al. (U.S. Patent No. 6,656,801).

In regards to claim 8, Applicant's Prior Art fails to disclose the following:

a) an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors.

However, Summerfelt discloses a semiconductor device that has an element isolation insulating film (8) formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has an element isolation insulating film formed on the surface of said semiconductor device and isolating a plurality of element regions, wherein each element region includes two transistors out of said plurality of transistors as disclosed in Summerfelt because it aids in separating the transistors source/drains (For Example: See Paragraph 29).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

b) the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor.

However, Corvasce discloses a semiconductor device that has the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has the line connecting the source and the drain of one of said two transistor is substantially orthogonal to the line connecting the source and the drain of the other one of said two transistor as disclosed in Corvasce because it aids in providing minimal cell size (For Example: See Abstract).

Additionally, since Applicant's Prior Art and Corvasce are both from the same field of endeavor, the purpose disclosed by Corvasce would have been recognized in the pertinent art of Applicant's Prior Art.

In regards to claim 10, Applicant's Prior Art fails to disclose the following:

a) the other one of the source or the drain of said transistor is shared by said two transistors in each element region.

However, Summerfelt discloses a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region (For Example: See Figure 1A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Applicant's Prior Art to include a semiconductor device that has the other one of the source or the drain of said transistor is shared by said two transistors in each element region as disclosed in Summerfelt because it aids in reducing the capacitance (For Example: See Paragraphs 7 and 8).

Additionally, since Applicant's Prior Art and Summerfelt are both from the same field of endeavor, the purpose disclosed by Summerfelt would have been recognized in the pertinent art of Applicant's Prior Art.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

December 10, 2005